



Version with Markings for Specification  
Application Serial No. 09/434,985  
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## LOW NOISE FULL INTEGRATED MULTILAYER[[S]] MAGNETIC FOR POWER CONVERTERS

### Related Applications

This is a continuation of United States Patent application serial number 08/351,943, filed  
5 on December 8, 1994, and entitled "Low Noise Full Integrated Multilayer Magnetic for Power  
converters[[.]]," incorporated herein by reference.

### Field of the Invention

This invention relates to DC-to-DC converters, DC-to-AC, AC-to-AC and AC-to-DC  
converters. The major characteristics of this power conversion technique is are that all the  
10 magnetic elements are implemented on the same multilayer[[s]] structure, ~~and~~ the power transfer  
is made highly efficient and ~~by minimizing the common mode noise~~ is minimized.

### Background of the Invention

There is a continuing industry demand for increasing power density, which means more  
power transferred in a given volume. A method for increasing the power transfer through the  
15 converter is to increase the switching frequency in order to minimize the size of ~~magnetic~~  
magnetics and the capacitors. Using prior art topologies such as forward or flyback, which  
employ "hard" switching techniques, makes high frequency operation less efficient. The  
switching losses associated with switch elements, which turn on when there is a voltage across  
them, are proportional with the switching frequency. An increase in switching frequency leads  
20 to an increase in switching losses and an increase in level of electromagnetic interference (EMI).

In order to overcome limitations in switching speeds, the prior art has devised a new  
family of resonant and quasi-resonant converters. In the case of quasi-resonant converters, the  
prior art technique consists of shaping the current or voltage to become half-sinusoidal and to  
perform the switching when the current or voltage reaches zero. The reactive elements, which  
25 contribute to shaping the current or voltage, are part of the basic circuit and are considered  
undesirable in classic topologies. An example of one such circuit can be found in Vinciarelli,

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"Forward Converter Switching at Zero Current," U.S. Patent No. 4,415,959. The technique utilized by Vinciarelli consists of adding a resonant capacitor across the fly wheeling diode to create a resonant circuit in combination with the leakage inductance of the transformer. During the ON time of the main switch, a current charges the resonant capacitor. When the current reaches zero, the main switch turns OFF in the primary of the transformer. The output inductor discharges the resonant capacitor, transferring the energy to the load. This topology exhibits several drawbacks which limit its utilization to power under 200W.

~~An other~~ Another family of quasi-resonant converters which switch at zero voltage is described by F. C. Lee in ~~high~~ High Frequency Power Conversion International Proceedings (April 1987), Intertec Communications, Ventura, California. These prior art circuits operate similarly to those described above with the exception that the main switch turns ON and OFF at zero voltage. ~~This has~~ Despite the advantage this has at ~~across~~ the main switch, ~~and~~ the frequency modulation which is required for controlling the output power makes this topology unattractive.

New topologies ~~structures~~ which are referred to as "Soft ~~transitions~~ Transition Technologies" were developed, in order to eliminate the limitations associated with ~~Quasi-resonant~~ quasi-resonant and resonant converters, but to still maintaining the advantage of soft commutations for the switching elements. Such technologies are described by ~~Mr. I.~~ Jitaru in "Fixed Frequency Single Ended Forward Converter Switching at Zero Voltage," U.S. Patent ~~[[#]]~~ No. 5,126,931, and in "Square Wave Converter ~~having~~ Having an Improved Zero Voltage Switching Operations," U.S. Patent ~~[[#]]~~ No. 5,231,563. Using these topologies the converter operates at constant frequency, modulating the power by varying the duty cycle, the current and voltages on the switching elements are square-wave to decrease the current and voltages stress, the transitions are done at zero voltage conditions, and the power is transferred to the output, both during the ON time and OFF time.

These latest topologies have proven superior in respect of efficiency over the previous resonant, and quasi-resonant topologies ~~have proven superior in respect of efficiency over the previous resonant topologies~~. However, the parasitic elements of the circuit, such as leakage inductance and stray inductance, will negatively affect the efficiency due the circulating energy contained in these parasitic elements. Due to the ~~inter-winding~~ inter-winding capacitance of the

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transformer the common mode noise will be injected into the secondary. In planar, low profile ~~magnetic~~ magnetics required for low profile packaging the inter-winding capacitance is larger, and as a result the common mode noise injected via ~~these~~ parasitic capacitance is larger.

### Brief Summary of the Invention

5        ~~The~~ Power processing devices according to this invention offer[[s]] a construction technique of the main transformer which also extends to all the magnetic elements, wherein the parasitic elements of the circuit are minimized. ~~In~~ At the same time the common mode current injected to the secondary via the ~~inter-winding~~ inter-winding capacitance is reduced and even eliminated. The construction technique ~~elaimed~~ provided in the power processing devices of this invention[[s]] offers a simple and low cost method ~~in~~ to further ~~suppressing~~ suppress the differential and common mode noise at the converter level. This novel construction technique offers an avenue ~~in~~ to increasing the power density of the converter and allows full compliance with the requirements of safety agencies.

15        The planar multilayer[[s]] magnetic is characterized by the use of flat copper spirals located on separate dielectric layers. Each layer can contain one turn or multiple spiral turns. The interconnection between the layers can be done by vias or an interconnecting ~~heater~~ trace. The insulator material can be laminated epoxy filled board, such as FR4 or a different dialectic material[[s]]. The planar multilayer[[s]] structure has been described by ~~Mr. Alex A.~~ Estrov in "Power Transformer Design for 1Mhz Resonant Converter" at High Frequency Power

20        Conversion in 1986. However, by decreasing the height of the planar magnetic the footprint will increase ~~inn~~ in order to maintain the same winding resistance. This will sacrifice the power density of the converter. In the exemplary embodiment of power processing devices according to this invention the transformer winding is ~~winding~~ is buried between a minimum of two layers of dialectic and the space ~~in~~ on top of the winding can be populated with surface mounted

25        components for a better volumetric efficiency. The Exemplary devices in accordance with the invention ~~elaims~~ provide several winding structures in a planar transformer, designed to minimize the common mode noise. The ~~inventions~~ exemplary embodiments further ~~elaims~~ provide a full integrated multilayer[[s]] structure in which all the magnetic elements are located

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on the same multilayer[[s]] structure. The winding arrangements in the input and output inductor are also structures to minimize the common mode noise. It further utilizes the ~~inter-layers~~ inter-layer capacitance to create a low impedance for the common mode and differential mode noise, and to short it back to the source. To compensate for the common mode noise injected by the primary switching elements into the common baseplate to the secondary, the power processing devices according to the invention ~~claims~~ provide a noise cancellation technique by ~~injected~~ injecting into the secondary a common mode current of the same amplitude, but in opposite phase, through the common baseplate or through the multilayer structure. In certain exemplary embodiments of ~~The~~ the invention ~~claims~~ a packaging configuration[[s]] is provided in which some of the components of the converter are surface mounted, located on the same multilayer[[s]] structure, and for higher power applications, cuts in the multilayer[[s]] structure ~~are performed~~ to allow for the body of the power components. The heat-sink of the power components may be connected to external heat-sinks.

### Brief Description of the Drawings

Figure 1 is a fragmentary cross-section view of the buried multilayer[[s]] magnetic for a better volumetric efficiency.

Figure 2 is a top plan view ~~if the of an~~ assembled power converter using ~~full~~ fully integrated multilayer[[s]] magnetic.

Figure 3A is a view of an inner layer in the fully integrated multilayer magnetic which contains a section of an input filter choke winding, a section of a transformer's primary winding and a section of the output choke core.

Figure 3B is a view of an inner layer in the full integrated multilayer[[s]] magnetic which contains a section of the input ~~filter~~ choke winding, a section of the transformer's secondary winding and a section of the output choke ~~inductor~~ winding.

Figure 4 is a schematic diagram of a power conversion device that depicts the injection of the common mode current through the primary to a secondary winding capacitance, due to the voltage gradient across the primary winding of the transformer.

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Figure 5 is a schematic diagram of the power conversion device like that of Fig. 4 that  
~~presents~~ illustrates the effect of a shield between primary and secondary winding in order to  
decrease common mode current via the primary to secondary winding capacitance.

Figure 6 is a schematic diagram of a power conversion device that ~~presents~~ illustrates the  
use of a differential mode and common mode input choke together with two “Y” capacitors in  
order to reduce the common mode current flowing towards the input source.

Figure 7 is a schematic illustration of ~~presents~~ a typical “sandwich” layer distribution in  
the transformer for a reduced leakage inductance and a reduced ac copper losses.

Figure 8 is a schematic illustration of ~~depicts~~ a layer and winding distribution aimed to  
decreased the common mode current injection to the secondary, by locating the secondary layers  
in between “quiet” primary layers. Quiet primary windings are those which exhibit a lower  
amplitude voltage swing in report to the primary ground.

Figure 9 is a schematic illustration of ~~presents~~ a further layer and winding distribute for  
common mode current reduction by using a shield between the secondary and two “quiet”  
primary layers.

Figure 10 is a schematic illustration of a further layer and winding distribution that  
~~presents~~ provides a method for the cancellation of the common mode current into the secondary  
by locating the secondary layers between the a “quiet” layer winding connected to the input DC  
voltage source and a “~~Noise~~ noise cancellation winding” which creates a negative imagine of the  
common mode current injected by the first layer.

Figure 11 is a schematic illustration of a configuration in which the secondary windings  
are located between two symmetrical auxiliary windings, which are wound in a such way to  
cancel the common mode current injected to the secondary via the primary to secondary winding  
capacitance.

Figure 12 is a schematic illustration of a configuration in which the switching element is  
connected in the middle of the primary winding, creating a perfect symmetry in which the  
common mode current injected into the secondary winding via the primary to secondary  
capacitance is canceled.

Figure 13 is a diagrammatic illustration of ~~depicts~~ a winding arrangement in a magnetic  
element designed to reduce the inter-winding capacitance and for a better utilization of the

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copper. ~~The width of each turns becomes larger as one moves from the inside turn to the outermost turn. In this way the winding resistance for the shorter turn can equal to the winding resistance for the longer turn. There is a shift between the layers to minimize the capacitance in between two adjacent layers.~~

5           Figure 14 is a fragmentary diagrammatic illustration of a construction using ~~presents a~~ method of compliance with IEC950 in which ~~with~~ three layers of core material are used, for example FR4, between the primary winding and secondary winding.

              Figure 15 is a fragmentary diagrammatic illustration of a construction using ~~presents a~~ second method of compliance with IEC950 wherein the core material ~~in~~ between primary and  
10           secondary winding has to be thicker than .4mm.

              Figure 16 is a fragmentary diagrammatic illustration of a construction using ~~depicts a~~ method of compliance with safety agencies in which the magnetic core is reported to the primary and the transformer does not have to be buried. The secondary winding has to comply with the creepage distances in accordance with coating environment, based on the RMS voltages  
15           measured in the transformer.

              Figure 17 is a schematic illustration of ~~presents a~~ configuration in which multiple multilayer[[s]] transformers on the same multilayer[[s]] structure are utilized for higher power applications or for a reduced number of layers.

### Detailed Description of the Preferred Embodiments

20           The multilayer[[s]] planar magnetic, in which the windings are continuous flat copper spirals located on separate dielectric substrates, have been used before for signal and data processing. In the power conversion filed field the multilayer[[s]] magnetic ~~started to be have been~~ been used since 1986. However, there are several limitations with multilayer[[s]] magnetic which prevented this technology from a large utilization. Decreasing the height of the magnetic,  
25           by utilizing flat windings, leads to an increased footprint. As a result a large portion of the board on which the multilayer[[s]] planar magnetic is mounted, cannot be used for another purpose, having a negative impact on the volumetric efficiency. Another limitation associated with planar multilayer[[s]] magnetic is the increased ~~inter-winding~~ inter-winding capacitance, which leads to

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higher switching losses on the switching elements and a larger common mode current injected to the secondary via the capacitance between primary and secondary windings. The parasitic elements such as the leakage inductance can be decreased in planar multilayer technology, but there is still the negative effect of parasitic elements associated with the interconnection pins.

5 The interconnection pins will add to the cost of the magnetic and also will contribute[[d]] an increase in losses.

~~This~~ Turning now to Fig. 1 wherein a methodology of the invention is illustrated. The planar windings of the magnetic [[8]] 18 are incorporated in a[[n]] multilayer[[s]] PCB structure 16. The top and bottom layer of the multilayer[[s]] board 16 are utilized for interconnection and

10 for pads of power components 20, or for shielding purposes or different other interconnections. By burying the magnetic winding inside of the multilayer[[s]] construction the footprint of the magnetic is reduced to the footprint of the core. ~~this will~~ This allows a better utilization of the board, increasing also the power density. By burying the magnetic inside of [[a]] an epoxy filled multilayer[[s]] structure such as the multilayer[[s]] PCB, the creepage distances requirement ~~in~~

15 between the windings and the edge of the board or cuts ~~will be~~ is decreased. This is due to the fact that the spacing between primary and secondary inside of the multilayer[[s]] PCB has to comply with the coating environment. These spacings are several times smaller than those in the air.

Another advantage of this construction technique is the fact that the ~~inter-connection~~

20 interconnection between the magnetic elements, for example between the transformer and output choke are done through the same multilayer[[s]] PCB, eliminating the need for ~~inter-connection~~ interconnection pins. The power components can be located ~~in on~~ on top of the multilayer[[s]] PCB, interconnecting with the magnetic winding through vias, or can be located on an external heatsink, using cuts in the PCB tailored to the body of power components as is depicted in Fig. 2.

25 In Fig. 2 is presented a ~~full~~ fully integrated multilayer[[s]] PCB power converter structure which incorporates all the magnetic elements such as the input filter 10, the main transformer 12, and the output choke 14. The body of the power components is accommodated by using cuts in the multilayer[[s]] PCB structure. The connection of power components to the windings is done by through holes in which the terminals of the components can be soldered ~~to~~. For lower power

30 levels the power components are located ~~in~~ on top of the PCB and through vias or large parallel

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pads ~~a set~~ of low thermal impedance extended to the bottom of the multilayer[[s]] PCB to which an external heatsink can be attached. The additional heatsink may not be required if there is an air flow ~~in-on~~ top of the converter.

The magnetic core 18 ~~will have its~~ has legs penetrating through the multilayer[[s]] PCB.

5 The core will create a closed magnetic path with or without an air gap, as a function of the electrical topology in which it is utilized.

In ~~figure~~ Fig. 3A ~~is presented~~ the structure of an inner layer ~~which~~ contains a section of the input choke winding 22 and a section of the primary winding 24 of the transformer. The cores of the input choke 10, main transformer 12 and output choke 14, ~~are penetrating~~ penetrate  
10 through the multilayer[[s]] PCB. The vias 26, are designed to interconnect the windings from different layers. Some of the vias are designed to interconnect the magnetic windings to the components located on the top and bottom of the multilayer[[s]] PCB.

In ~~figure~~ Fig. 3B ~~is presented~~ the structure of an inner layer is shown which ~~contained~~ contains [[a]] another section of the input choke winding 22, a section of the secondary winding  
15 28 of the transformer 28 and a section of the winding 30 of the output choke 30. The connection from the transformer to output choke is done directly without supplementary interconnections. This will minimize the stray inductance associated with the interconnection pins.

One of the ~~novelty claimed by~~ novel aspects of this invention is the integration of all the magnetic elements on the same multilayer[[s]] structure. ~~for a~~ For better utilization of ~~the~~ space,  
20 the magnetic windings are buried inside, allowing the top and bottom layer to be utilized for locating surface mounted components. This leads to a very efficient utilization of the volume due to a three dimensional utilization. This form of integration leads to a minimization of the interconnection impedance and as result leads to a higher efficiency in power processing. The available area on the board of Figs. 3A and 3B is the area on the top and bottom surfaces not  
25 taken up by the footprints of the cores 10, 12 and 14 and thus available for mounting circuit components. Mounting components directly above or below the footprints of the windings 22, 24, 28 and 30 and their end connection pads in the embodiment of Figs. 3A and 3B frees up  
slightly more than 30% of the available area for this purpose. Using this real estate on the top and/or bottom surfaces of the multilayer PCB thus enables greatly improving the converter's  
30 power density. In a converter like that depicted in Figs. 3A and 3B in excess of 25% of the

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surface of the board (the total area inside the perimeter of the board) is made unavailable by the magnetic cores 10, 12 and 14. If the winding footprints are excluded from the area to be populated by surface mounted circuit components then the real estate on surfaces of the board that can be used to mount these components is reduced by nearly half.

5           The multilayer[[s]] PCB magnetic offers a good avenue in addressing the creepages and clearance requirements demanded by the safety agencies. By ~~burring~~ burying the transformer inside of the PCB as is depicted in ~~fig~~ Fig. 14, the spacing between primary and secondary is determined in accordance with the RMS voltages in transformer applied to a coating environment. These spacing are several times smaller than those in the air. However, between  
 10   primary and secondary windings two or three layers of core material 92, 94, 96 is are demanded, each two able to withstand the dielectric test. Another method requires the core material between the primary and secondary 98, to be at least .4mm. The magnetic core can be reported to the primary or to the secondary. In Fig. 16 an exemplary embodiment is shown ~~presented-a~~  
 15   ~~ease~~ in which the core is reported to the primary. The secondary windings 104 are buried inside and the distance from the secondary winding 104 to the edge of the core slow has to comply with the creepage requirements for the RMS voltage measured in the transformer. Using this method the primary winding 102 and the interconnecting vias do not have to be buried in the multilayer[[s]] PCB.

          The AC voltage gradient across each turn of the winding is equal, but reported to the  
 20   input ground the amplitude of the voltage swing increases from the turn connected to the input DC source to the maximum level to the turn connected to the switching element. As is depicted in Fig. 4, the voltage swing 32 across the primary winding[,] injects a current in the secondary winding 38 via the primary to secondary winding capacitance 34, 36. This current is further flowing through the decoupling capacitor 40, through the earth ground 44, returning through the  
 25   connections of the input and output leads of the power supply and is a noise parameter that is measured by the FCC and VDE.

As depicted in Fig. 5, One one method in of suppressing some of the common ~~node mode~~ (CM) noise is utilizing a shield 54, or two located ~~in~~ between primary and secondary winding and connected to the input DC source or the input ground. ~~The method is depicted in Fig.5.~~ The  
 30   capacitance between the shield 54 and the primary winding creates a low impedance path for the

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common mode current created by the AC voltage across the primary winding 32. However the stray impedance of the shield itself will create a voltage gradient across it which will inject a common mode current via the capacitance 56 between the shield and the secondary winding 38. This common mode current 42, is reduced in comparison to the structure without the shield.

5 However, the parasitic inductance of the connection to the input DC source 46, is critical for shielding effectiveness. One of the major drawback associated with the use of the shield is the fact that an increased parasitic capacitance will be created across the primary winding and across the secondary winding. This will increase the switching losses on the switching elements. This parasitic capacitance 52 will be in parallel with the ~~inter-winding~~ inter-winding capacitance of  
10 the primary and the parasitic capacitance of the switch itself. The switching losses will become more significant at higher operation frequency and for high input voltage applications such as ~~Off-line~~ off-line converters.

In Fig. 7, ~~is presented in~~ a winding arrangement in a converter, in which the secondary windings 80 are sandwiched between the primary windings. For simplicity, I consider that the  
15 primary winding of the transformer is contained in four layers and the secondary winding is one layer. The winding of layer 1 connected to the input voltage source 72, exhibits a lower voltage swing reported to the input ground comparative to the winding 78 of layer 4 connected to the switching element 70. In this particular case the voltage swing reported to the primary ground is four times larger for layer 4, 78 than for the layer 1, 72. It is logical to locate the secondary 80 in  
20 the vicinity of the "quiet" primary such as 72. However the secondary has to be located symmetrically ~~in~~ between primary windings for two reasons. One reason is to minimize the magnetic field intensity ~~in~~ between windings for lower AC copper loss, and the second reason is to lower the leakage inductance between primary and secondary.

In order to decrease the common mode current injection into the secondary via the  
25 capacitance between primary winding to secondary winding, and maintaining ~~in~~ at the same time the sandwiched structure, the configuration of Fig. 8 is suggested. In Fig. 8 the secondary winding is located between two "~~Quiet~~" quiet layers. The voltage swing across layer 1 is much smaller than the voltage swing across layer 3. This structure does not eliminate the common mode injection to the secondary but it will reduce it. The advantage of this configuration is the  
30 fact that it does not require any addition layer.

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In ~~Figure Fig. 9~~ is ~~presented~~ a configuration in which two layers ~~in~~ on the top and the bottom of the secondary are used as a shield 54. The location of the shield in vicinity of two "quiet" layers, layer 1, 72 and 2, 74, will not increase significantly the parasitic capacitance across the primary winding. However two layers of the multilayer[[s]] structure will be allocated  
5 to the shield 54.

A configuration which can reduce the common mode noise injection to the secondary to zero is depicted in Fig. 10. In this configuration a noise cancellation winding 82, is added. The polarity of the voltage swing across this winding is ~~in~~ opposite to the polarity of the voltage swing across the ~~wining~~ winding in a layer 1. As a result the common mode current injected into  
10 the secondary winding will be canceled. This method will require only one additional layer and if a perfect geometrical symmetry can be accomplished, the common mode current injected in the secondary can be totally canceled. The single drawback of this is the fact that one layer will be allocated just for the noise cancellation.

In ~~Figure Fig. 11~~ is ~~presented~~ a configuration in which two layers are added, one ~~in~~ on top and one ~~in~~ on the bottom of the secondary winding. ~~This~~ These windings have a common symmetrical connection which is connected to the input ground. The connection can be also to the input DC voltage source. The voltage swing across the winding 1, 84 and auxiliary winding 2, 86 will inject a common mode current into the secondary, but of the opposite polarity of each other. As a result the total common mode current injected to the secondary will be zero. These  
15 20 auxiliary windings can be utilized to provide power in the primary section such as the necessary bias power, or can provide the power for the primary reported output.

Another path for the common mode current is through the capacitance between the switching elements in the primary and in the secondary, and the baseplate. This applies for higher power applications in which a common heatsink baseplate is used for the power  
25 components in the primary and secondary circuits. Due to a large voltage swing of the power switch tab, this source of common mode noise can be dominant. This invention claims a method for cancellation of the common mode current produced by the switching elements. This is done by creating a supplementary capacitor between the secondary and the termination of the noise cancellation winding not connected to the input DC source or input ground. The noise  
30 cancellation windings are ~~described~~ shown in Fig. 10 and Fig. 11. By properly tailoring this

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additional capacitance a current will be injected into the secondary, of the same amplitude but in opposite phase to the current injected by the switching elements to the secondary via the capacitance between the switches and the baseplate. The additional capacitance between the noise cancellation winding and secondary can be implemented in the metal baseplate or in the multilayer[[s]] structure.

Another method which does not require supplementary layers for output common mode noise cancellation is presented in ~~figure~~ Fig. 12. In this case the primary winding is symmetrically cut in [[a]] half and the power switch is connecting to these sections. The voltage swing on the layers which surrounds the secondary, layer 2, 74 and layer 3, 76, will have the same amplitude but will be of opposite polarity. As a result the common mode noise injected into the secondary will be zero.

The structures presented above will reduce the common mode noise injection to the secondary via the ~~inter-winding~~ inter-winding capacitance of the transformer. However, if the common mode noise will be generated by different circuitry or if a further reduction of common mode is required, a supplementary common mode filter may be required. Such a structure is ~~described~~ shown in Fig. 6. By utilizing a EE or EI core gapped in the center leg, the input choke can exhibit a common mode and a differential mode impedance. By using the outer legs of the ~~Encore~~ core, two inductive elements can be implemented in the PCB. The coupling ~~in~~ between these inductor will determine the CM impedance, and it can be tailored by the ~~gaping~~ gapping configuration of the core. For example, if there is not a gap in the core, the coupling coefficient is  $K=.071$ . If there is 1 mill gap in all the legs,  $K=.276$ . If only the center leg is ~~gaped~~ gapped to 2 mil,  $K=.724$ . The common mode and differential mode inductance can be tailored by properly gapping the core, and making sure that under all loading conditions the core does not saturate. Utilizing full integrated multilayer[[s]] PCB, the cost of the input EMI filter is reduced to the cost of the magnetic core. The capacitors 62, and 64 are used to ~~erate~~ create a low impedance for the common mode current which will work against the high impedance exhibited by the input filter. The capacitors 62 and 64 can be created in the structure of the multilayer[[s]] ~~PBC~~ PCB, which will lead to a cost ~~reductio~~ reduction of the converter and to a better utilization of the multilayer[[s]] structure. These capacitors can be constructed to comply with the safety agencies

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by using the recommendations suggested for the transformer compliance with safety agencies, previously discussed.

~~In figure Fig. 13 is presented a method for~~ provides reduction of the parasitic capacitance across the magnetic winding. This is accomplished by shifting the adjacent layers. For a better utilization of the copper, the turn width ~~will vary~~ is varied in such a way to ensure an equal resistance per each turn. The turn width is made larger as one moves from the inside turn to the outermost turn so that the winding resistance for the shorter turn can be equal to the winding resistance for the longer turn. For higher power applications or in applications which require large currents multiple planar multilayer[[s]] transformers can be utilized on the same multilayer[[s]] structure as ~~in~~ is depicted in Fig. 17. The number of layers in primary 112, 114, 116 and in the secondary 118, 120, 122 of these transformers 106, 120, 122 can be reduced to one, which will allow the use of two layer multilayer[[s]] structure. Another advantage of this configuration is the fact that the leakage inductance in each transformer can be very low, which will make this configuration ideal for high current and low output voltage.

Many alternations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. ~~therefore~~ Therefore, the invention must be understood as being set forth above only for the purpose of example and not by way of limitation. The invention is defined by the following claims wherein means may be substituted therein for obtaining substantially the same result even when not obtained by performing substantially the same function in substantially the same way.